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AMENDMENT TO THE CLAIMS

1. (Previously Presented) A transistor device comprising:

a source;

a drain;

a gate; and

a p-type hole metal channel having a thickness of less than 5 nm with the channel being positioned relative to the gate such that the carriers in the channel are controlled by the gate.

2. (Original) The device of Claim 1 further comprising an insulating layer and a gate insulator, the metal channel being positioned between the gate insulator and the insulating layer.

3. (Original) The device of Claim 1 further comprising a silicon substrate.

4. (Original) The device of Claim 1 wherein the metal channel comprises a continuous thin conductive film having a thickness less than 5 nm.

5. (Original) The device of Claim 1 wherein the metal channel has a thickness in a range of 0.2 to 3 nm.

6. (Original) The device of Claim 1 wherein the transistor comprises an enhancement mode device.

7. (Original) The device of Claim 1 wherein the transistor comprises a depletion mode device.

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8. (Previously Presented) A field effect transistor device comprising:

an n-type metal channel formed over an insulator, the metal channel further comprising a continuous thin conductive film having a thickness less than 5 nm, and wherein the n-type metal is a material selected from the group consisting of a pure metal, a combination of metals including alloy, doped metals, layered metals, or metallic materials including conductive silicides, conductive salicides and conductive nitrides;

a source including a p-type material and a drain including a p-type material; and

a gate and a gate insulator formed over the channel, the gate controlling carriers in the channel.

9. (Original) The device of Claim 8 wherein the insulator further comprises an insulating layer over a substrate, the metal channel being positioned between the gate and the insulating layer and the gate insulator being positioned under the gate and over the metal channel.

10. (Original) The device of Claim 8 further comprising a silicon substrate.

11. (Cancelled)

12. (Original) The device of Claim 8 wherein the device further comprises a complementary transistor device.

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13. (Original) The device of Claim 8 further comprising an encapsulation layer.

14. (Original) The device of Claim 8 wherein the metal channel has a length in a range of 5 nm to 50 nm and a width in a range of 50 nm to 500 nm.

15. (Original) The device of Claim 8 wherein the channel comprises a plurality of layers.

16. (Previously Presented) The device of Claim 1 wherein a type of carriers within the metal channel is controlled by the gate.

17. (Previously Presented) The device of Claim 1 wherein the source comprises a p-type metal and the drain comprises a p-type metal, and wherein the metal channel is a p-type metal that is sufficiently thin that the number of carriers within the metal channel can be controlled by a gate to form a p-channel depletion-mode device.

18. (Previously Presented) The device of Claim 1 wherein the source comprises an n-type metal and the drain comprises an n-type metal; and wherein the metal channel comprises a p-type metal such that an n-type inversion layer is formed on the p-type metal upon application of sufficient positive gate voltage to form an n-channel enhancement-mode device.

19. (Previously Presented) The device of Claim 1 wherein the device further comprises a transistor of opposite conductivity type on a common substrate to form a complementary circuit.

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20. (Previously Presented) The device of Claim 1 wherein the channel comprises a plurality of layers.

21. (Previously Presented) The device of Claim 1 wherein the metal channel comprises a metal alloy, doped metal, metal silicide, metal salicide or metal nitride.

22. (Previously Presented) The device of claim 8, further comprising a p-type inversion layer.

23. (Previously Presented) The device of claim 8, wherein a p-type inversion layer is formed on the n-type metal upon application of a negative gate voltage.

24. (Cancelled)

25. (Previously Presented) The device of claim 23, wherein a thickness of the n-metal layer is greater than a thickness of the p-type inversion layer.

26. (Previously Presented) The device of claim 23 wherein the p-type inversion layer is on a first side of the n-type metal to form a p-channel enhancement-mode device.

27-35 (Cancelled)

36. (New) A transistor device comprising:

a source;

a drain;

a gate; and

a p-type hole metal channel having a thickness of less than 5 nm with the channel being positioned relative to the gate such

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that the carriers in the channel are controlled by the gate, the metal channel comprising a material selected from the groups consisting of a pure metal, a doped metal, a metal alloy, a conductive metal silicide, a conductive metal salicide and a conductive metal nitride.

37. (New) The device of Claim 36 further comprising an insulating layer and a gate insulator, the metal channel being positioned between the gate insulator and the insulating layer.

38. (New) The device of Claim 36 wherein the transistor comprises an enhancement mode device.

39. (New) The device of Claim 36 wherein the transistor comprises a depletion mode device.

40. (New) A field effect transistor device comprising:

an n-type metal channel formed over an insulator, the metal channel further comprising a material selected from the group consisting of a pure metal, a metal alloy, a doped metal, layered metals, or metallic materials including conductive silicides, conductive salicides and conductive nitrides;

a source including a p-type material and a drain including a p-type material; and

a gate and a gate insulator formed over the channel, the gate controlling carriers in the channel.

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